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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES
Docket No. 13398US02

In the Application of:

Alexander G. MacInnis, et al.

Serial No.: 10/786,195

Filed: February 25, 2004

For: SIMD SUPPORTING FILTERING IN A VIDEO DECODING SYSTEM

Examiner: David H. Malzahn

Group Art Unit: 2193

Conf. No.: 2398

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John A. Wiberg
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BRIEF ON APPEAL

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Sir:

This is an appeal from an Office Action dated December 7, 2007, in which claims 1-27 were finally rejected.

REAL PARTY IN INTEREST

Broadcom Corporation, a corporation organized under the laws of the state of California, and having a place of business at 5300 California Avenue, Irvine, California 92617, has acquired the entire right, title and interest in and to the invention, the application, and any and all patents to be obtained therefor, as set forth in the Assignment recorded at Reel 014620, Frame 0542 in the PTO assignment search room.

10/07/2008 VBUI11 00000013 130017 10786195
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RELATED APPEALS AND INTERFERENCES

There currently are no appeals pending regarding related applications.

STATUS OF THE CLAIMS

Claims 1-27 are pending in the present application. Pending claims 1-27 stand rejected and are the subject of this appeal.

STATUS OF THE AMENDMENTS

None.

SUMMARY OF CLAIMED SUBJECT MATTER

Claim 1 is directed to a media processing filter engine operable to perform filtering operations on an input data stream comprising blocks of media data. The filter engine includes a first memory unit, a second memory unit, and a single instruction, multiple data (SIMD) processor. The first and second memory units store blocks of media data to be processed. The SIMD processor receives blocks of media data from the first and second memory units and simultaneously performs filtering operations on blocks of media data from the first and second memory units.

The invention of claim 1 is illustratively described in the Specification of the present application at, for example, paragraphs [28]-[38], referring to Figure 2. FIG. 2 shows a first memory unit X1 (204), a second memory unit X0 (206), and a single instruction, multiple data (SIMD) processor 200. The X1 and X0 memory units store blocks of media data to be processed. The SIMD processor 200 receives blocks of media data from the X1 and X0 memory units and simultaneously performs filtering operations on blocks of media data from the X1 and X0 memory units.[1] The invention of claim 1 is also described in other parts of the application, such as in the Summary of the Invention section.

Claims 2-9 are dependent upon claim 1.

[1] See, e.g., Specification, paragraph [0029], lines 1-2.

Claim 10 is directed to a media processing filter engine adapted to perform filtering operations on an input data stream comprising blocks of media data. The filter engine includes a first memory unit, a second memory unit, a first shift register, a second shift register, and a processor. The first and second memory units store blocks of media data to be processed. The first shift register receives and stores blocks of media data from the first memory unit. The second shift register receives and stores blocks of media data from the second memory unit. The first and second shift register each selectively shift their contents by a predetermined number of bits corresponding to the size of a data element. The processor receives blocks of media data from the first and second shift registers and simultaneously performs filtering operations on blocks of media data from the first and second shift registers.

The invention of claim 10 is illustratively described in the Specification of the present application at, for example, paragraphs [28]-[39], [49], [51] and [52], referring to Figures 2, 3 and 7. FIG. 2 shows a first memory unit X1 (204), a second memory unit X0 (206), and a single instruction, multiple data (SIMD) processor 200. The X1 and X0 memory units store blocks of media data to be processed. Figure 7 shows a first shift register Z1 (602) and a second shift register Z0 (604). Shift register Z1 receives and stores blocks of media data from the X1 memory unit.[2] Shift register Z0 receives and stores blocks of media data from the X0 memory unit.[3] The first shift register Z1 and the second shift register Z0 each selectively shift their contents by a predetermined number of bits corresponding to the size of a data element.[4] The shift registers Z1 and Z0 provide media data to the data processing units 4-7 (702) and data processing units 0-3 (704), which are part of the SIMD processor 200.[5] The SIMD processor 200 simultaneously performs filtering operations on blocks of media data from the shift registers Z1 and Z0, and thus from the X1 and X0 memory units.[6] The invention of claim 10 is also described in other parts of the application, such as in the Summary of the Invention section.

Claims 11-18 are dependent upon claim 10.

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[2] Specification, paragraph [0051], lines 3-4.
[3] Specification, paragraph [0051], lines 4-5.
[4] Specification, paragraph [0049], lines 7-10.
[5] Specification, paragraph [0051], lines 6-9.
[6] See, e.g., Specification, paragraph [0029], lines 1-2.

Claim 19 is directed to a media processing filter engine adapted to perform filtering operations on an input data stream comprising blocks of media data. The filter engine includes a first memory unit, a second memory unit, a first shift register, a second shift register, and a processor. The first and second memory units store blocks of media data to be processed. The first shift register receives and stores blocks of media data from the first memory unit. The second shift register receives and stores blocks of media data from the second memory unit. The first and second shift register each selectively shift their contents by a predetermined number of bits corresponding to a multiple of the size of a data element. The processor receives blocks of media data from the first and second shift registers and simultaneously performs filtering operations on blocks of media data from the first and second shift registers.

The invention of claim 19 is illustratively described in the Specification of the present application at, for example, paragraphs [28]-[39], [49], [51] and [52], referring to Figures 2, 3 and 7. FIG. 2 shows a first memory unit X1 (204), a second memory unit X0 (206), and a single instruction, multiple data (SIMD) processor 200. The X1 and X0 memory units store blocks of media data to be processed. Figure 7 shows a first shift register Z1 (602) and a second shift register Z0 (604). Shift register Z1 receives and stores blocks of media data from the X1 memory unit.[7] Shift register Z0 receives and stores blocks of media data from the X0 memory unit.[8] The first shift register Z1 and the second shift register Z0 each selectively shift their contents by a predetermined number of bits corresponding to a multiple of the size of a data element.[9] The shift registers Z1 and Z0 provide media data to the data processing units 4-7 (702) and data processing units 0-3 (704), which are part of the SIMD processor 200.[10] The SIMD processor 200 simultaneously performs filtering operations on blocks of media data from the shift registers Z1 and Z0, and thus from the X1 and X0 memory units.[11] The invention of claim 10 is also described in other parts of the application, such as in the Summary of the Invention section.

Claims 20-27 are dependent upon claim 19.

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[7] Specification, paragraph [0051], lines 3-4.
[8] Specification, paragraph [0051], lines 4-5.
[9] Specification, paragraph [0049], lines 7-10.
[10] Specification, paragraph [0051], lines 6-9.
[11] See, e.g., Specification, paragraph [0029], lines 1-2.

GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

I. Claims 1-27 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent 5,659,780 issued to Chen-Mie Wu.

ARGUMENT

I. Claims 1-27 are not anticipated under 35 U.S.C. § 102(b) by Wu (US 5,659,780).

In the Office Action of December 7, 2007, claims 1-27 were rejected under 35 U.S.C. § 102(b) as being anticipated by Wu (US 5,659,780). 35 U.S.C. 102(b) states:

> A person shall be entitled to a patent unless... the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.[12]

To anticipate a claim, the reference must teach every element of the claim. "A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference."[13]

A. Claims 1-9 are not anticipated under 35 U.S.C. § 102(b) by Wu (US 5,659,780).

Claim 1 is directed to

> 1. A media processing filter engine operable to perform filtering operations on an input data stream comprising blocks of media data, the filter engine comprising:
>
> a first memory unit to store blocks of media data to be processed;
>
> a second memory unit operable to store blocks of media data to be processed; and
>
> a single instruction, multiple data (SIMD) processor operable to receive blocks of media data from the first and second memory units and to simultaneously perform filtering operations on blocks of media data from the first and second memory units.

Claim 1 is distinguishable from Wu for several reasons. The Examiner asserts that the multiport memory M of Wu constitutes first and second memory elements per

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[12] 35 U.S.C. 102(b)

[13] *Verdegaal Bros. v. Union Oil Co. of California*, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

claim 1. This interpretation is directly at odds with Figure 1 of Wu and its supporting text, which clearly shows and describes the mutiport memory M is a single memory unit.[14] Therefore, the processor shown in Figure 1 of Wu does not receive blocks of data from first and second memory units in accordance with claim 1. Appellant made this argument in the Amendment filed on October 22, 2007.[15] In response to this argument, in the Office Action of December 7, 2007, the Examiner argued, "Contrary to applicant's remarks Wu's multi-port memory may be view a (sic) multiple memory units."[16] Appellant disagrees and submits that Wu's multiport memory M is shown and described as a single memory unit, not as first and second memory units as claimed in claim 1 and as described in the specification of the present application. Therefore, claim 1 is not anticipated by Wu.

Furthermore, claim 1 specifies that it is directed to a media processing filter engine. Claim 1 also specifies that the first memory unit stores blocks of *media* data, that the second memory element stores blocks of *media* data, and that the SIMD processor receives blocks of *media* data from the first and second memory units and performs filtering operations on the blocks of *media* data. Appellant submits that Wu does not teach these aspects of claim 1. Therefore, Appellant submits that claim 1, and claims 1-9 depending thereon, are not anticipated by Wu.

[14] U.S. Patent 5,659,780, Figure 1 and column 3, line 21 – column 5, line 6.
[15] Amendment filed October 22, 2007, page 11.
[16] Office Action mailed December 7, 2007, page 2, last paragraph.

B. Claims 10-18 are not anticipated under 35 U.S.C. § 102(b) by Wu (US 5,659,780).

Claim 10 is directed to:

> 10. A media processing filter engine adapted to perform filtering operations on an input data stream comprising blocks of media data, the filter engine comprising:
>
> a first memory unit operable to store blocks of media data to be processed;
>
> a second memory unit operable to store blocks of media data to be processed;
>
> a first shift register operable to receive and store blocks of media data from the first memory unit, wherein the first shift register is adapted to selectively shift its contents by a predetermined number of bits corresponding to the size of a data element;
>
> a second shift register operable to receive and store blocks of media data from the second memory unit, wherein the second shift register is operable to selectively shift its contents by a predetermined number of bits corresponding to the size of a data element; and
>
> a processor operable to receive blocks of media data from the first and second shift registers and to simultaneously perform filtering operations on blocks of media data from the first and second shift registers.

Claim 10 includes limitations that are similar to those included in claim 1. Appellant submits that claim 10 is not anticipated by Wu for the reasons set forth above with respect to claim 1. Furthermore, Wu does not teach that the shift registers rs11-rs1n and rs21-rs2n selectively shift their contents by a predetermined number of bits corresponding to the size of a data element per claim 10. The Examiner alleges that Wu teaches this aspect of claim 10, but fails to point out where Wu does so. Therefore, Appellant submits that claim 10, and claims 11-18 depending thereon, are not anticipated by Wu.

C. Claims 19-27 are not anticipated under 35 U.S.C. § 102(b) by Wu (US 5,659,780).

Claim 19 is directed to:

> 19. A media processing filter engine adapted to perform filtering operations on an input data stream comprising blocks of media data, the filter engine comprising:
>
> a first memory unit operable to store blocks of media data to be processed;
>
> a second memory unit operable to store blocks of media data to be processed;
>
> a first shift register operable to receive and store blocks of media data from the first memory unit, wherein the first shift register is adapted to selectively shift its contents by a predetermined number of bits corresponding to a multiple of the size of a data element;
>
> a second shift register operable to receive and store blocks of media data from the second memory unit, wherein the second shift register is operable to selectively shift its contents by a predetermined number of bits corresponding to the size of a data element; and
>
> a processor operable to receive blocks of media data from the first and second shift registers and to simultaneously perform filtering operations on blocks of media data from the first and second shift registers.

Claim 19 includes limitations that are similar to those included in claims 1 and 10. Appellant submits that claim 19 is not anticipated by Wu for the reasons set forth above with respect to claims 1 and 10. Furthermore, Wu does not teach that the shift registers rs11-rs1n and rs21-rs2n selectively shift their contents by a predetermined number of bits corresponding to a multiple of the size of a data element per claim 19. Therefore, Appellant submits that claim 19, and claims 20-27 depending thereon, are not anticipated by Wu.

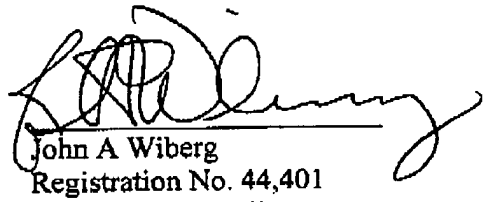
II. Conclusion

For at least the foregoing reasons, Appellant submits that claims 1-27 are not anticipated by Wu. Reversal of the Examiner's rejection and issuance of a patent on the application are therefore requested.

The Commissioner is hereby authorized to charge $540 (to cover the Brief on Appeal Fee of $510) and any additional fees or credit any overpayment to the deposit account of McAndrews, Held & Malloy, Account No. 13-0017.

Dated: October 6, 2008

Respectfully submitted,



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APPENDIX

(37 C.F.R. § 1.192(c)(9))

The following claims are involved in this appeal:

1. A media processing filter engine operable to perform filtering operations on an input data stream comprising blocks of media data, the filter engine comprising:

a first memory unit to store blocks of media data to be processed;

a second memory unit operable to store blocks of media data to be processed; and

a single instruction, multiple data (SIMD) processor operable to receive blocks of media data from the first and second memory units and to simultaneously perform filtering operations on blocks of media data from the first and second memory units.

2. The filter engine of claim 1 wherein the SIMD processor is adapted to receive blocks of data from the first and second memory units, and to simultaneously perform filtering operations on blocks of data from the first and second memory units, when the filter engine is in a split-operation mode, and wherein when the filter engine is in a non-split-operation mode, the SIMD processor is adapted to receive blocks of data from only one of the first and second memory units, and to perform filtering operations on the received blocks of data.

3. The filter engine of claim 2 wherein when the filter engine is in the split-operation mode, the m most significant bits of a memory location of the first memory unit and the n most significant bits of a memory location of the second memory unit are provided to the SIMD processor, and the SIMD processor simultaneously performs filtering operations on the m most significant bits of the memory location of the first memory unit and the n most significant bits of the memory location of the second memory unit.

4. The filter engine of claim 3 wherein m and n are both equal to t/2, where t is the total number of bits in each of the memory locations of both the first and second memory units.

5. The filter engine of claim 1 wherein the SIMD processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and wherein the first set of data path units is adapted to perform filtering operations on a block of data received from the first memory unit while the second set of data path units is simultaneously performing filtering operations on a block of data received from the second memory unit.

6. The filter engine of claim 5 wherein, when the filter engine is in a split-operation mode, the first set of data path units performs filtering operations on a block of data received from the first memory unit while the second set of data path units simultaneously performs filtering operations on a block of data received from the second memory unit, and wherein when the filter engine is in a non-split-operation mode, both the first and second sets of data path units perform filter operations on blocks of data from only one of the first and second memory units.

7. The filter engine of claim 6 wherein when the filter engine is in the split-operation mode, the m most significant bits of a memory location of the first memory unit are provided to the first set of data path units and the n most significant bits of a memory location of the second memory unit are provided to the second set of data path units, and the first set of data path units performs filtering operations on the m most significant bits of the memory location of the first memory unit while the second set of data path units simultaneously performs filtering operations on the n most significant bits of the memory location of the second memory unit.

8. The filter engine of claim 7 wherein m and n are both equal to t/2, where t is the total number of bits in the memory locations of both the first and second memory units.

9. The filter engine of claim 1 adapted to perform filtering operations on an input data stream comprising blocks of video data, wherein:

the first memory unit is adapted to store blocks of pixel data to be processed;

the second memory unit is adapted to store blocks of pixel data to be processed; and

the SIMD processor is adapted to receive blocks of pixel data from the first and second memory units and to simultaneously perform filtering operations on blocks of pixel data from the first and second memory units.

10. A media processing filter engine adapted to perform filtering operations on an input data stream comprising blocks of media data, the filter engine comprising:

a first memory unit operable to store blocks of media data to be processed;

a second memory unit operable to store blocks of media data to be processed;

a first shift register operable to receive and store blocks of media data from the first memory unit, wherein the first shift register is adapted to selectively shift its contents by a predetermined number of bits corresponding to the size of a data element;

a second shift register operable to receive and store blocks of media data from the second memory unit, wherein the second shift register is operable to selectively shift its contents by a predetermined number of bits corresponding to the size of a data element; and

a processor operable to receive blocks of media data from the first and second shift registers and to simultaneously perform filtering operations on blocks of media data from the first and second shift registers.

11. The filter engine of claim 10 adapted to perform filtering operations on an input data stream comprising blocks of video data, wherein the first and second shift registers are adapted to selectively shift their contents by a predetermined number of bits corresponding to the size of one pixel.

12. The filter engine of claim 10 wherein the processor is adapted to receive blocks of data from the first and second shift registers, and to simultaneously perform filtering operations on blocks of data from the first and second shift registers, when the filter engine is in a split-operation mode, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and second memory units, and the processor is adapted to receive

blocks of data from the first shift register, but not from the second shift register, and to perform filtering operations on blocks of data from the first shift register.

13. The filter engine of claim 12 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register and the n most significant bits of the second shift register are provided to the processor, and the processor simultaneously performs filtering operations on the m most significant bits of the first shift register and the n most significant bits of the second shift register.

14. The filter engine of claim 13 wherein m and n are both equal to t/2, where t is the total number of bits that the processor is capable of simultaneously performing filtering operations on.

15. The filter engine of claim 10 wherein the processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and wherein the first set of data path units is adapted to perform filtering operations on a block of data received from the first shift register while the second set of data path units is simultaneously performing filtering operations on a block of data received from the second shift register.

16. The filter engine of claim 15 wherein, when the filter engine is in a split-operation mode, the first set of data path units performs filtering operations on a block of data received from the first shift register while the second set of data path units simultaneously performs filtering operations on a block of data received from the second shift register, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and second memory units, and both the first and second sets of data path units perform filter operations on blocks of data from the first shift register, but not from the second shift register.

17. The filter engine of claim 16 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register are provided to the

first set of data path units and the n most significant bits of the second shift register are provided to the second set of data path units, and the first set of data path units performs filtering operations on the m most significant bits of the first shift register while the second set of data path units simultaneously performs filtering operations on the n most significant bits of the second shift register.

18. The filter engine of claim 17 wherein m and n are both equal to t/2, where t is the total number of bits that the plurality of data path units are capable of simultaneously performing filtering operations on.

19. A media processing filter engine operable to perform filtering operations on an input data stream comprising blocks of media data, the filter engine comprising:

a first memory unit operable to store blocks of media data to be processed;

a second memory unit operable to store blocks of media data to be processed;

a first shift register adapted to receive and store blocks of media data from the first memory unit, wherein the first shift register is operable to selectively shift its contents by a predetermined number of bits corresponding to a multiple of the size of a data element;

a second shift register operable to receive and store blocks of media data from the second memory unit, wherein the second shift register is operable to selectively shift its contents by a predetermined number of bits corresponding to a multiple of the size of a data element; and

a processor operable to receive blocks of media data from the first and second shift registers and to simultaneously perform filtering operations on blocks of media data from the first and second shift registers.

20. The filter engine of claim 19 adapted to perform filtering operations on an input data stream comprising blocks of video data, wherein the first and second shift registers are adapted to selectively shift their contents by a predetermined number of bits corresponding to a multiple of the size of one pixel.

21. The filter engine of claim 19 wherein the processor is adapted to receive blocks of data from the first and second shift registers, and to simultaneously perform filtering operations on blocks of data from the first and second shift registers, when the filter engine is in a split-operation mode, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and second memory units, and the processor is adapted to receive blocks of data from the first shift register, but not from the second shift register, and to perform filtering operations on blocks of data from the first shift register.

22. The filter engine of claim 21 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register and the n most significant bits of the second shift register are provided to the processor, and the processor simultaneously performs filtering operations on the m most significant bits of the first shift register and the n most significant bits of the second shift register.

23. The filter engine of claim 22 wherein m and n are both equal to t/2, where t is the total number of bits that the processor is capable of simultaneously performing filtering operations on.

24. The filter engine of claim 19 wherein the processor comprises a plurality of data path units comprising a first set of data path units and a second set of data path units, and wherein the first set of data path units is adapted to perform filtering operations on a block of data received from the first shift register while the second set of data path units is simultaneously performing filtering operations on a block of data received from the second shift register.

25. The filter engine of claim 24 wherein, when the filter engine is in a split-operation mode, the first set of data path units performs filtering operations on a block of data received from the first shift register while the second set of data path units simultaneously performs filtering operations on a block of data received from the second shift register, and wherein when the filter engine is in a non-split-operation mode, the first shift register is adapted to receive and store blocks of data from one of the first and

second memory units, and both the first and second sets of data path units perform filter operations on blocks of data from the first shift register, but not from the second shift register.

26. The filter engine of claim 25 wherein when the filter engine is in the split-operation mode, the m most significant bits of the first shift register are provided to the first set of data path units and the n most significant bits of the second shift register are provided to the second set of data path units, and the first set of data path units performs filtering operations on the m most significant bits of the first shift register while the second set of data path units simultaneously performs filtering operations on the n most significant bits of the second shift register.

27. The filter engine of claim 26 wherein m and n are both equal to t/2, where t is the total number of bits that the plurality of data path units are capable of simultaneously performing filtering operations on.

EVIDENCE APPENDIX

Not applicable.

RELATED PROCEEDINGS APPENDIX

The Appellant is unaware of any related appeals or interferences.